**MOD N COUNTER**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity counter is

Port ( clk : in STD\_LOGIC;

count : out STD\_LOGIC\_VECTOR (3 downto 0));

end counter;

architecture Behavioral of counter is

signal s:std\_logic\_vector(3 downto 0):="0000";

--signal s1:std\_logic\_vector(20 downto 0):=(others=>'0');

signal sclk:std\_logic:='0';

begin

--process(clk)

--begin

--if(clk'event and clk='1')then

--s1<=s1+1;

--end if;

--end process;

--sclk<=s1(20);

process(clk)

begin

if(clk'event and clk='1')then

s<=s+1;

end if;

end process;

count<=s;

end Behavioral;